2 × 24 W BTL or 4 × 12 W single-ended car radio power amplifier

TDA8564Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use - Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8564Q is an integrated class-B output amplifier in a 17-lead DIL-bent-SIL power package. It contains 4 × 12 W single-ended or 2 × 24 W bridge amplifiers.

APPLICATIONS

- The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	4	A
$I_{q(tot)}$	total quiescent current		–	80	–	mA
I_{stb}	standby current		–	0.1	100	μA
Stereo BTL application						
P_o	output power	R_L = 4 Ω; THD = 10%	–	24	–	W
SVRR	supply voltage ripple rejection		–	41	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	200	–	μV
$\|Z_I\|$	input impedance		25	–	–	kΩ
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
Quad single-ended application						
P_o	output power	R_L = 4 Ω; THD = 10%	–	6.4	–	W
		R_L = 2 Ω; THD = 10%	–	12	–	W
SVRR	supply voltage ripple rejection		–	41	–	dB
V_{no}	noise output voltage	R_s = 0 Ω	–	200	–	μV
$\|Z_I\|$	input impedance		50	–	–	kΩ

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8564Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

BLOCK DIAGRAM

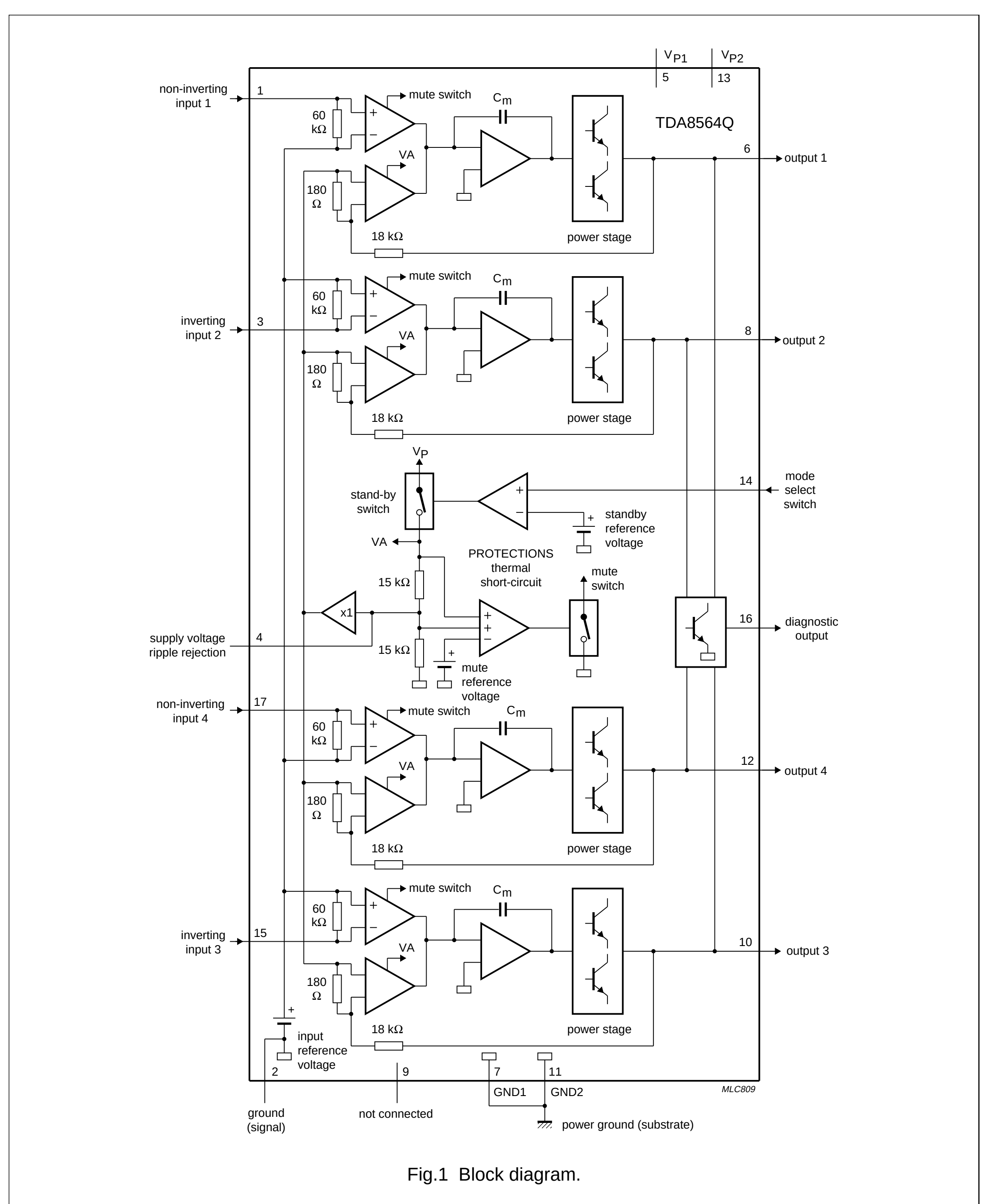


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
INV2	3	inverting input 2
SVRR	4	supply voltage ripple rejection
V_{P1}	5	supply voltage 1
OUT1	6	output 1
GND1	7	power ground 1
OUT2	8	output 2
n.c.	9	not connected
OUT3	10	output 3
GND2	11	power ground 2
OUT4	12	output 4
V_{P2}	13	supply voltage 2
MODE	14	mode select switch input
INV3	15	inverting input 3
V_{DIAG}	16	diagnostic output
–INV4	17	non-inverting input 4

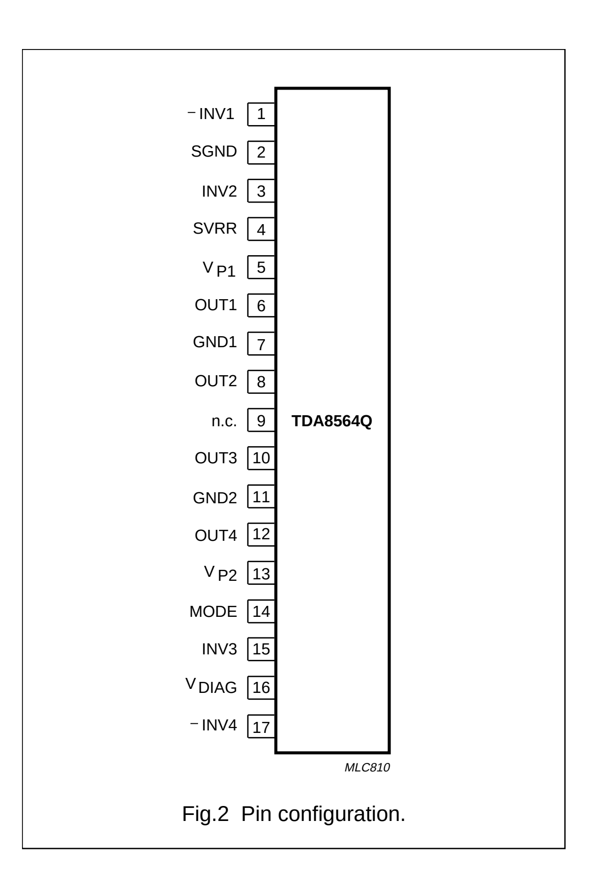


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8564Q contains four identical amplifiers which can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 40 dB (46 dB in BTL). Special features of the device are as follows.

Mode select switch (pin 14)

- Low standby current (<100 μA)
- Low switching current (low cost supply switch)
- Mute facility.

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥100 ms (charging of the input capacitors at pins 1, 3, 15 and 17).

This can be achieved by:

- Microcontroller control
- External timing circuit (see Fig.3).

The circuit in Fig.3 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

In the event of fast switching at mode select pin it is advised to increase the $\frac{1}{2}V_P$ decoupling capacitor (pin 4) to 150 μF to avoid switch plops.

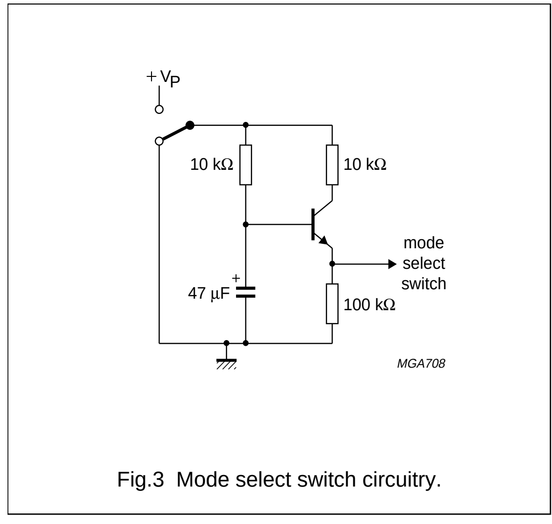


Fig.3 Mode select switch circuitry.

Diagnostic output (pin 16)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 16 goes LOW. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 16 is independent of the number of channels that are clipping (see Figs 4 and 5).

SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms after removal of the short-circuit. During this short-circuit condition, pin 16 is continuously LOW.

When a short-circuit across the load of one or more channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 µs to see whether the short-circuit is still present. Due to this duty cycle of 50 µs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 16 is LOW for 20 ms and HIGH for 50 µs (see Fig.6).

The power dissipation in any short-circuit condition is very low.

TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 16 will be active LOW.

OPEN-COLLECTOR OUTPUT

Pin 16 is an open-collector output, which allows pin 16 of more devices being tied together.

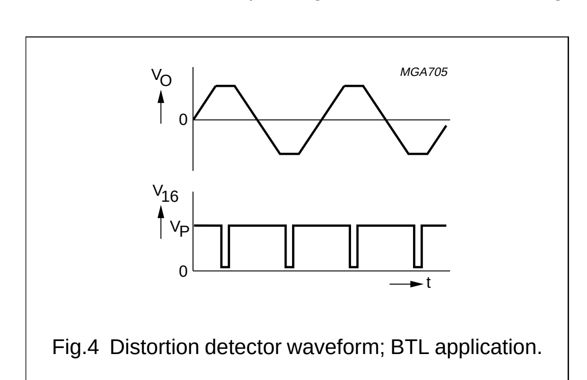


Fig.4 Distortion detector waveform; BTL application.

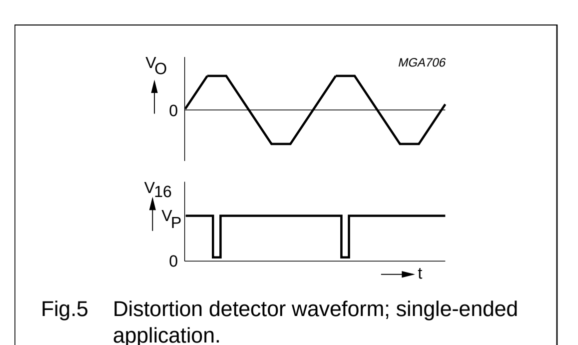


Fig.5 Distortion detector waveform; single-ended application.

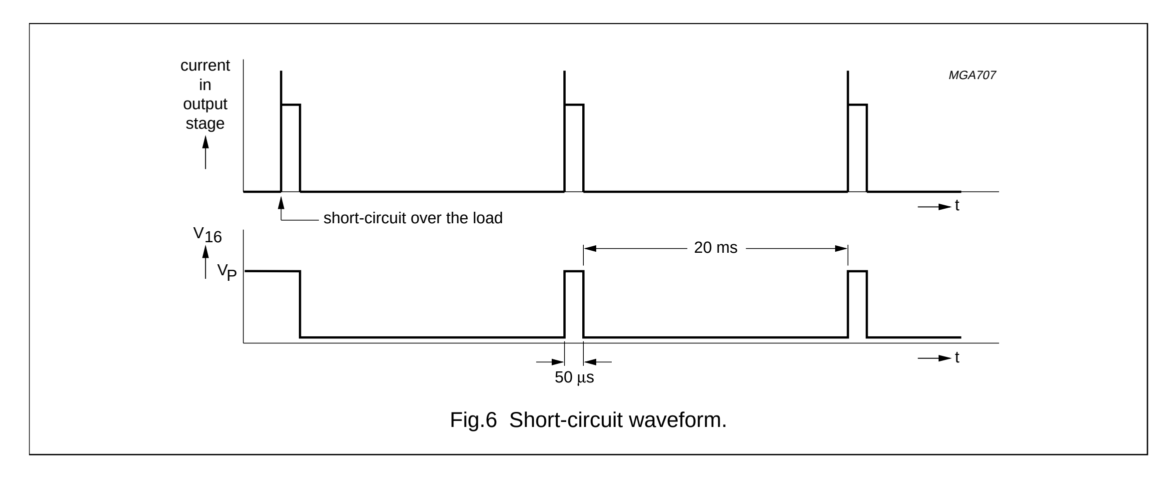


Fig.6 Short-circuit waveform.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage				
	operating		–	18	V
	non-operating		–	30	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	60	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	40	K/W
$R_{th\ j\text{-}c}$	thermal resistance from junction to case (see Figs 7 and 8)	1.3	K/W

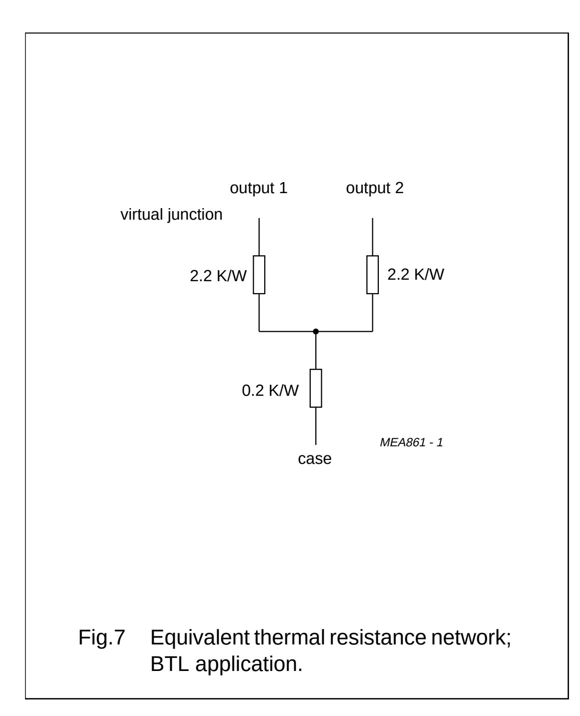


Fig.7 Equivalent thermal resistance network; BTL application.

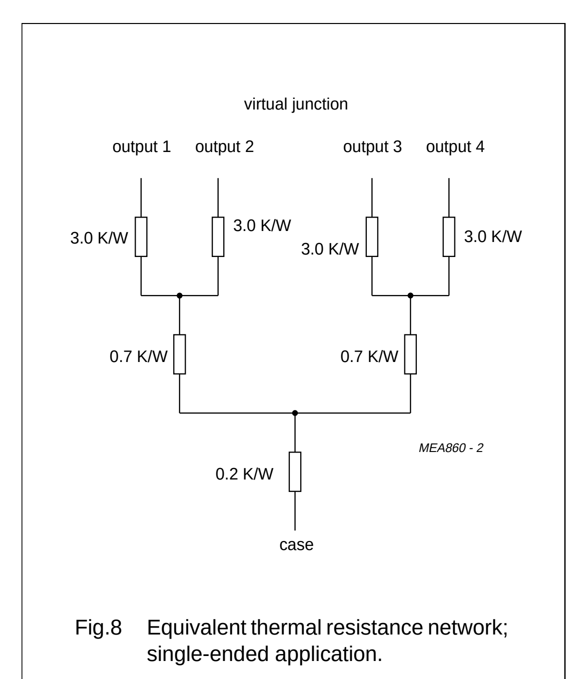


Fig.8 Equivalent thermal resistance network; single-ended application.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.17; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
I_q	quiescent current	see Fig.9	–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
Mute select switch						
V_{14}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output signal in mute position	$V_{I(max)}$ = 1 V; f = 1 kHz	–	–	20	mV
$\|\Delta V_O\|$	DC output offset voltage		–	–	250	mV
STANDBY CONDITION						
V_{stb}	DC voltage in standby condition		0	–	2	V
I_{stb}	DC current in standby condition		–	–	100	μA
I_{sw}	switch-on current		–	12	40	μA
Diagnostic output (pin 16)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

Notes

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.
2. At 18 V < V_P < 30 V the DC output voltage $\leq \frac{1}{2} V_P$.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (measured in Fig.17)						
P_o	output power	THD = 0.5%; note 1	15	19	–	W
		THD = 10%; note 1	20	24	–	W
P_o	output power	V_P = 13.2 V; THD = 0.5%; note 1	–	16	–	W
		V_P = 13.2 V; THD = 10%; note 1	–	20	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
f_{lr}	low frequency roll-off	at –1 dB; note 2	–	45	–	Hz
f_{hr}	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		45	46	47	dB
SVRR	supply voltage ripple rejection					
	on	note 3	38	41	–	dB
	mute	note 3	42	48	–	dB
	standby	note 3	80	–	–	dB
$\|Z_i\|$	input impedance		25	30	38	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	200	–	μV
	on	R_s = 10 kΩ; note 4	–	350	700	μV
	mute	notes 4 and 5	–	180	–	μV
α_{cs}	channel separation	R_s = 10 kΩ	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	V_{16} ≤ 0.6 V; no short-circuit	–	10	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Quad single-ended application (measured in Fig.18)						
P_o	output power	THD = 0.5%; note 1	4	5	–	W
		THD = 10%; note 1	5.5	6.4	–	W
P_o	output power	R_L = 2 Ω; THD = 0.5%; note 1	7.5	8.5	–	W
		R_L = 2 Ω; THD = 10%; note 1	10	12	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.15	–	%
f_{lr}	low frequency roll-off	at –3 dB; note 2	–	45	–	Hz
f_{hr}	high frequency roll-off	at –1 dB	20	–	–	kHz
G_v	closed loop voltage gain		39	40	41	dB
SVRR	supply voltage ripple rejection					
	on	note 3	38	41	–	dB
	mute	note 3	42	48	–	dB
	standby	note 3	80	90	–	dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_s = 0 Ω; note 4	–	200	300	μV
	on	R_s = 10 kΩ; note 4	–	250	–	μV
	mute	notes 4 and 5	–	175	–	μV
α_{cs}	channel separation	R_s = 10 kΩ	40	52	–	dB
$\|\Delta G_v\|$	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p).
4. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_s (V_I = 0 V).

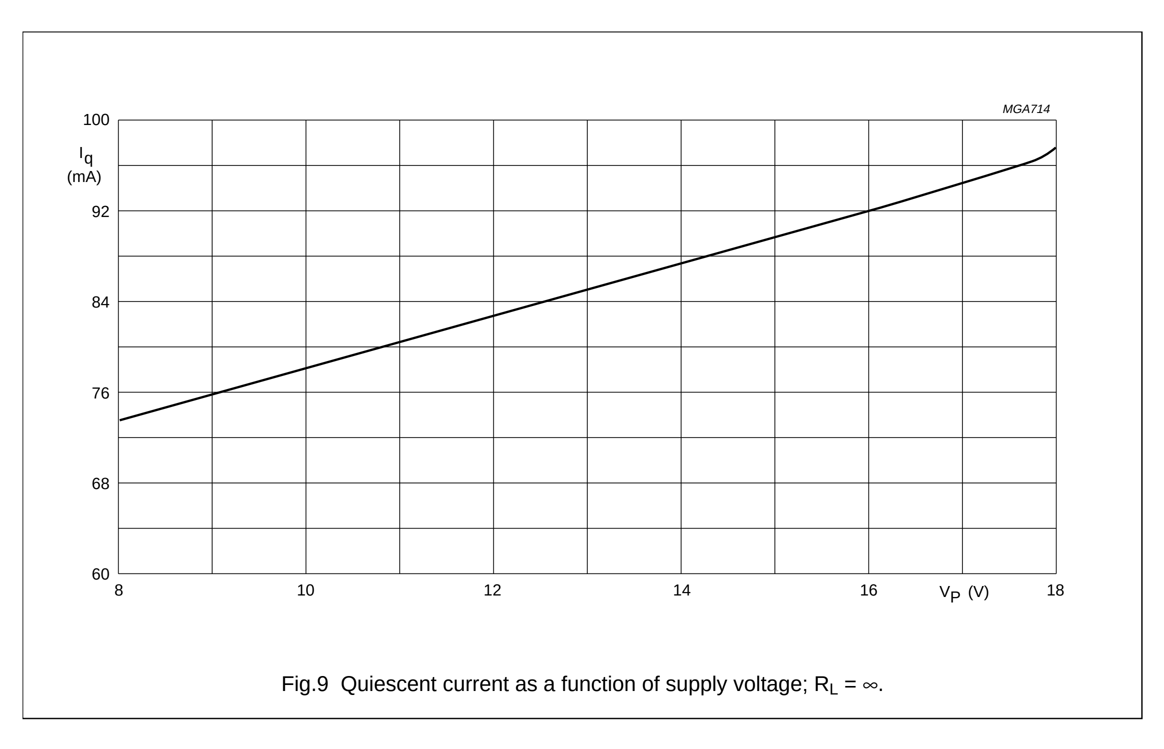
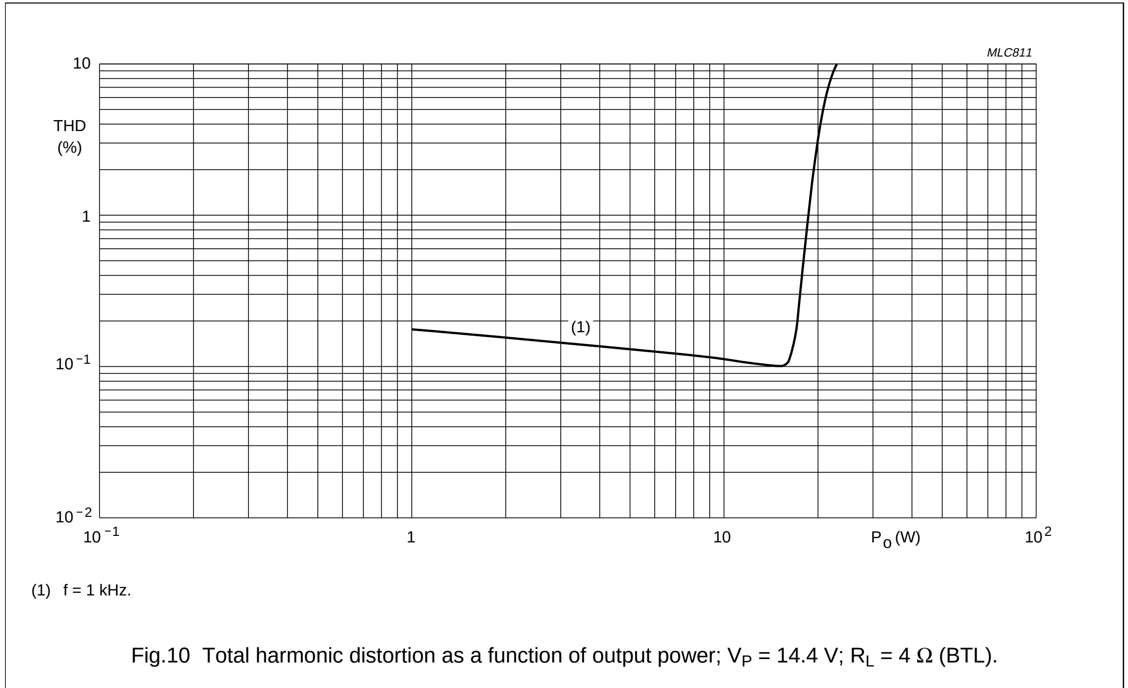
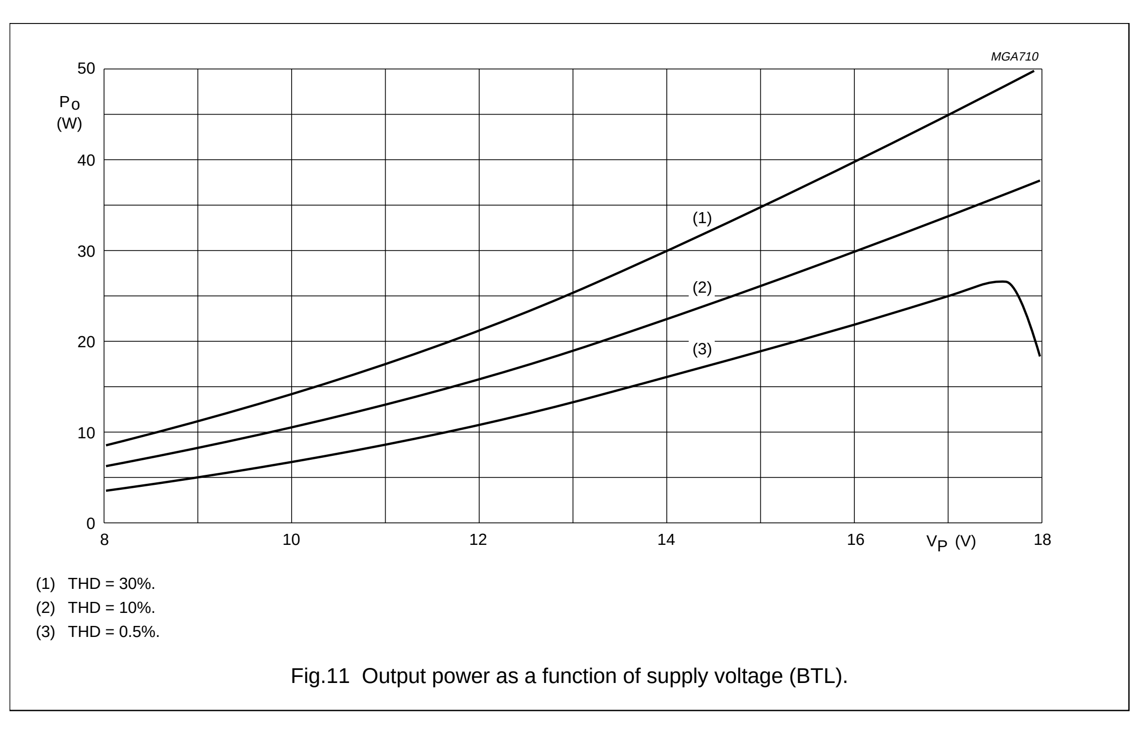


Fig.9 Quiescent current as a function of supply voltage; $R_L = \infty$.



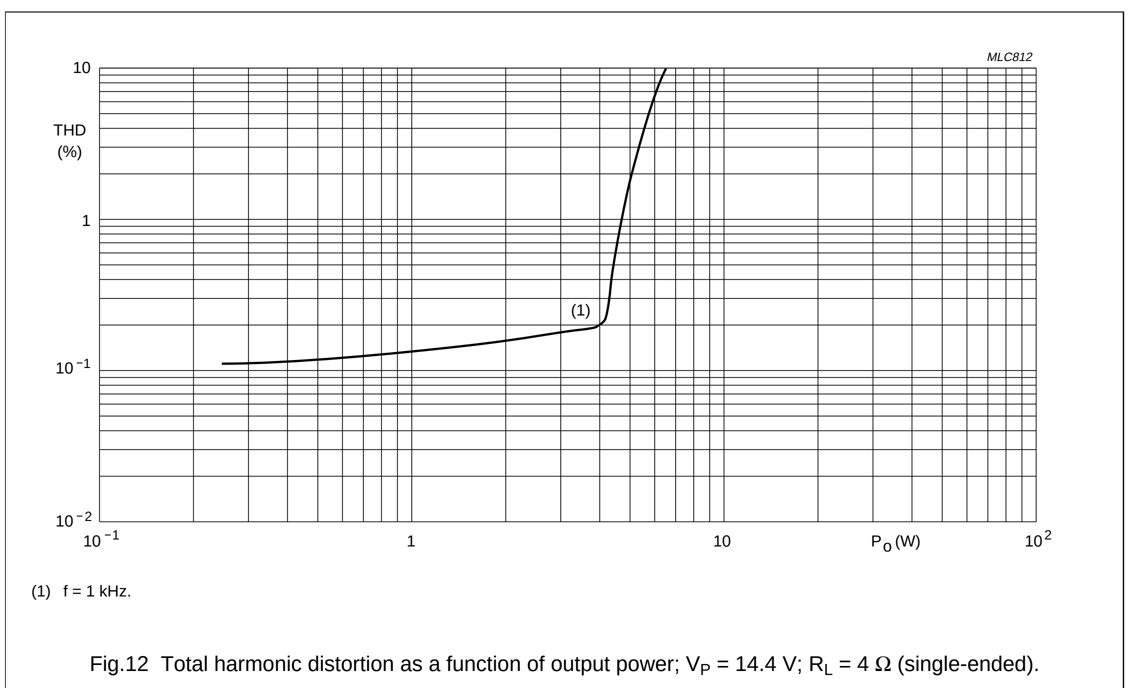
(1) f = 1 kHz.

Fig.10 Total harmonic distortion as a function of output power; V_P = 14.4 V; R_L = 4 Ω (BTL).



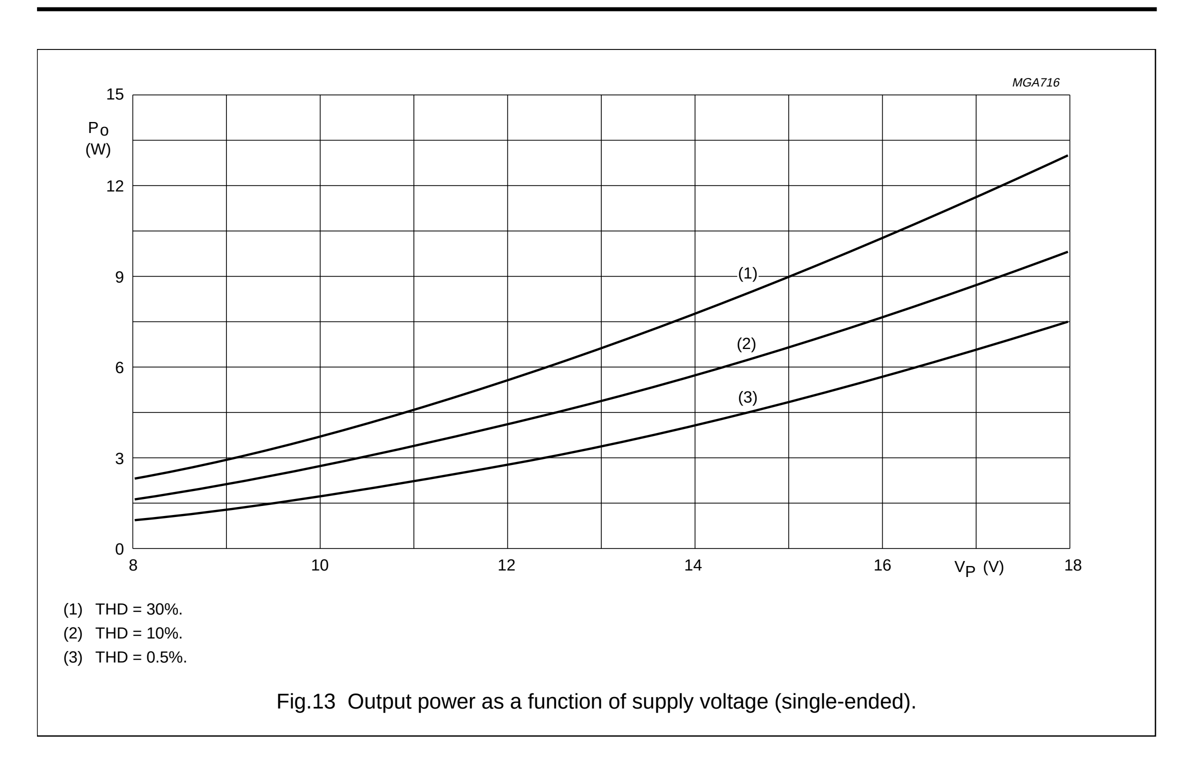
(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.11 Output power as a function of supply voltage (BTL).



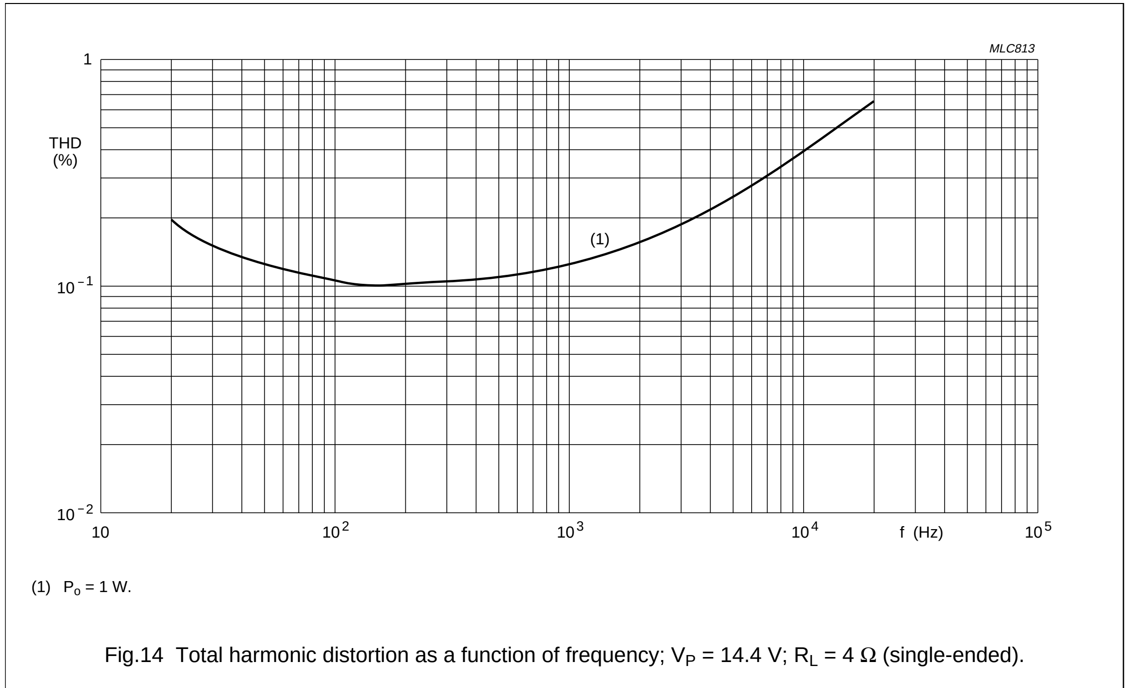
(1) f = 1 kHz.

Fig.12 Total harmonic distortion as a function of output power; V_P = 14.4 V; R_L = 4 Ω (single-ended).



(1) THD = 30%.
(2) THD = 10%.
(3) THD = 0.5%.

Fig.13 Output power as a function of supply voltage (single-ended).



(1) P_o = 1 W.

Fig.14 Total harmonic distortion as a function of frequency; V_P = 14.4 V; R_L = 4 Ω (single-ended).

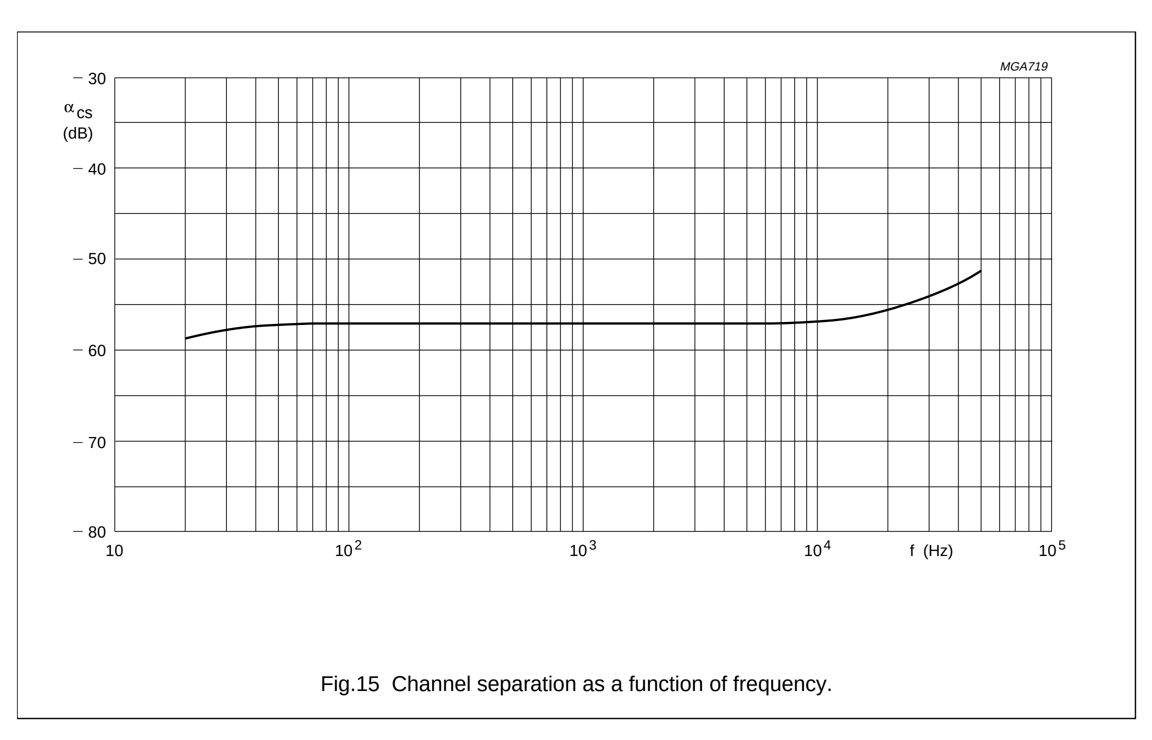
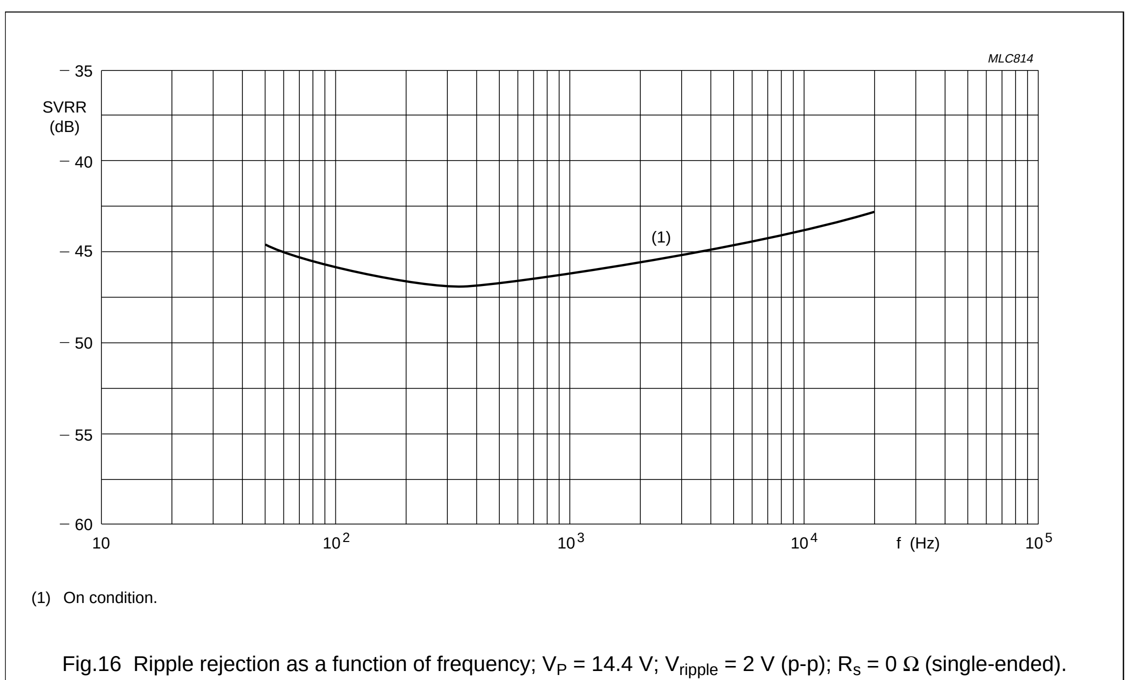


Fig.15 Channel separation as a function of frequency.



(1) On condition.

Fig.16 Ripple rejection as a function of frequency; V_P = 14.4 V; V_{ripple} = 2 V (p-p); R_s = 0 Ω (single-ended).

TEST AND APPLICATION INFORMATION

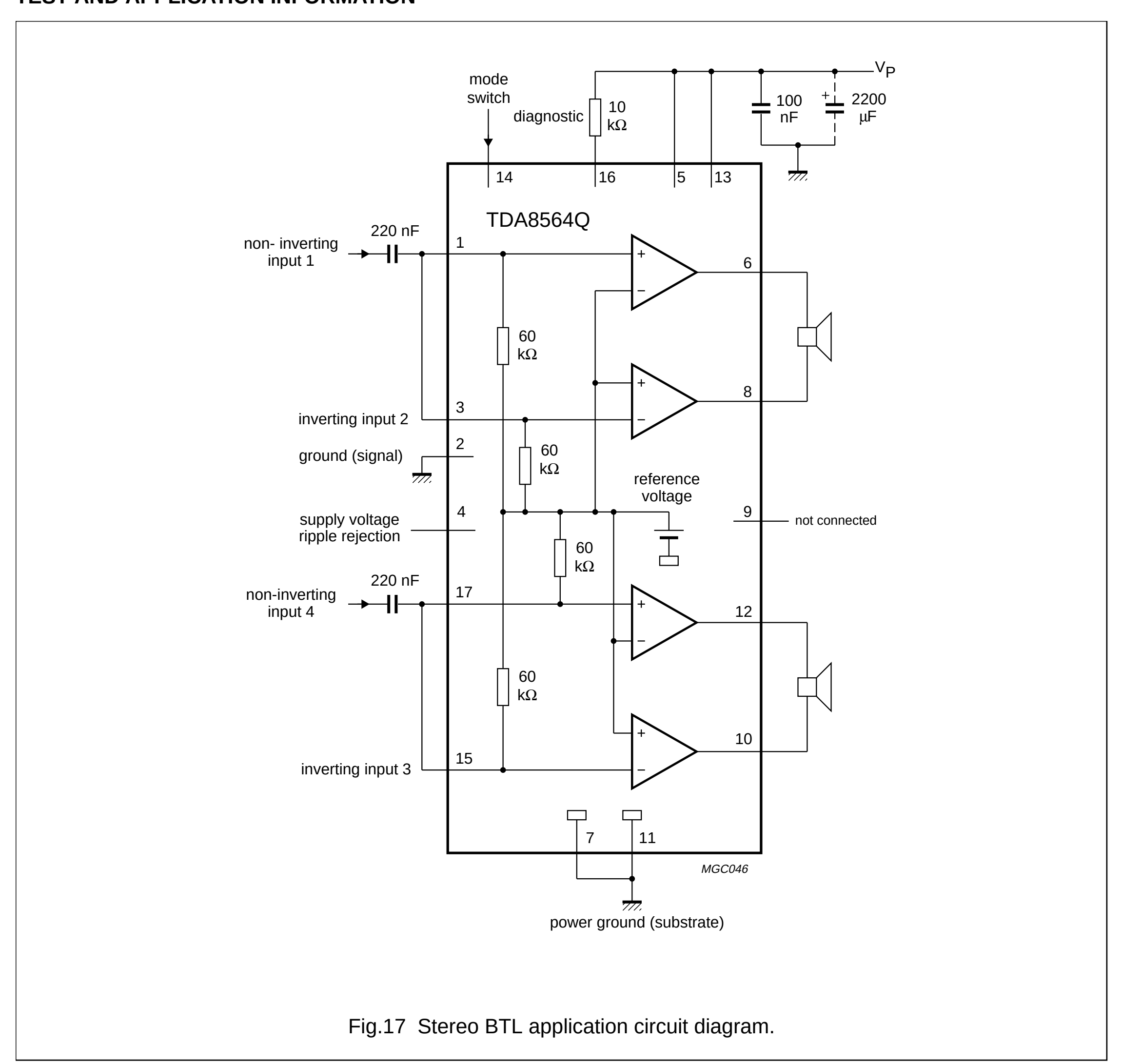


Fig.17 Stereo BTL application circuit diagram.

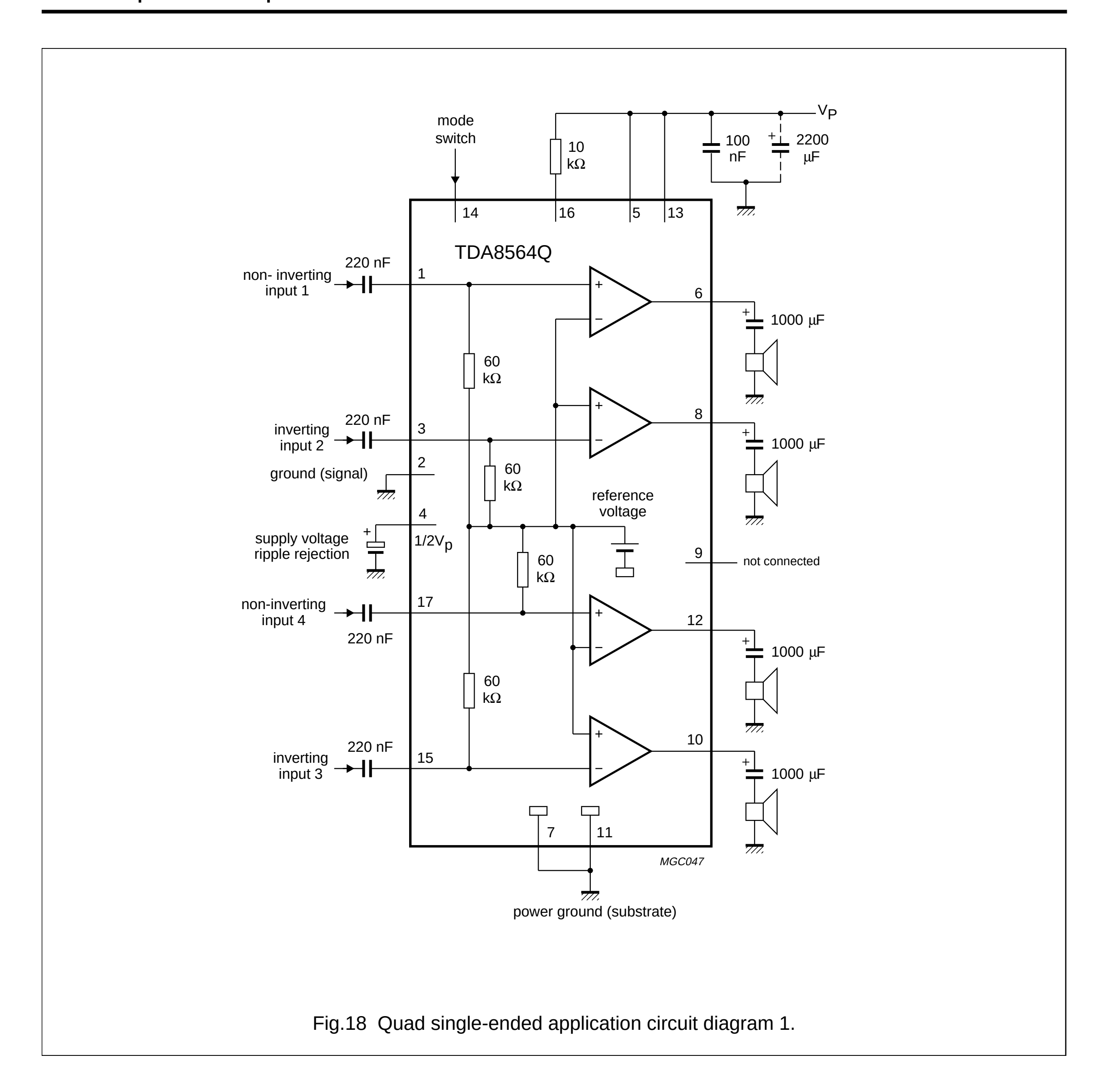
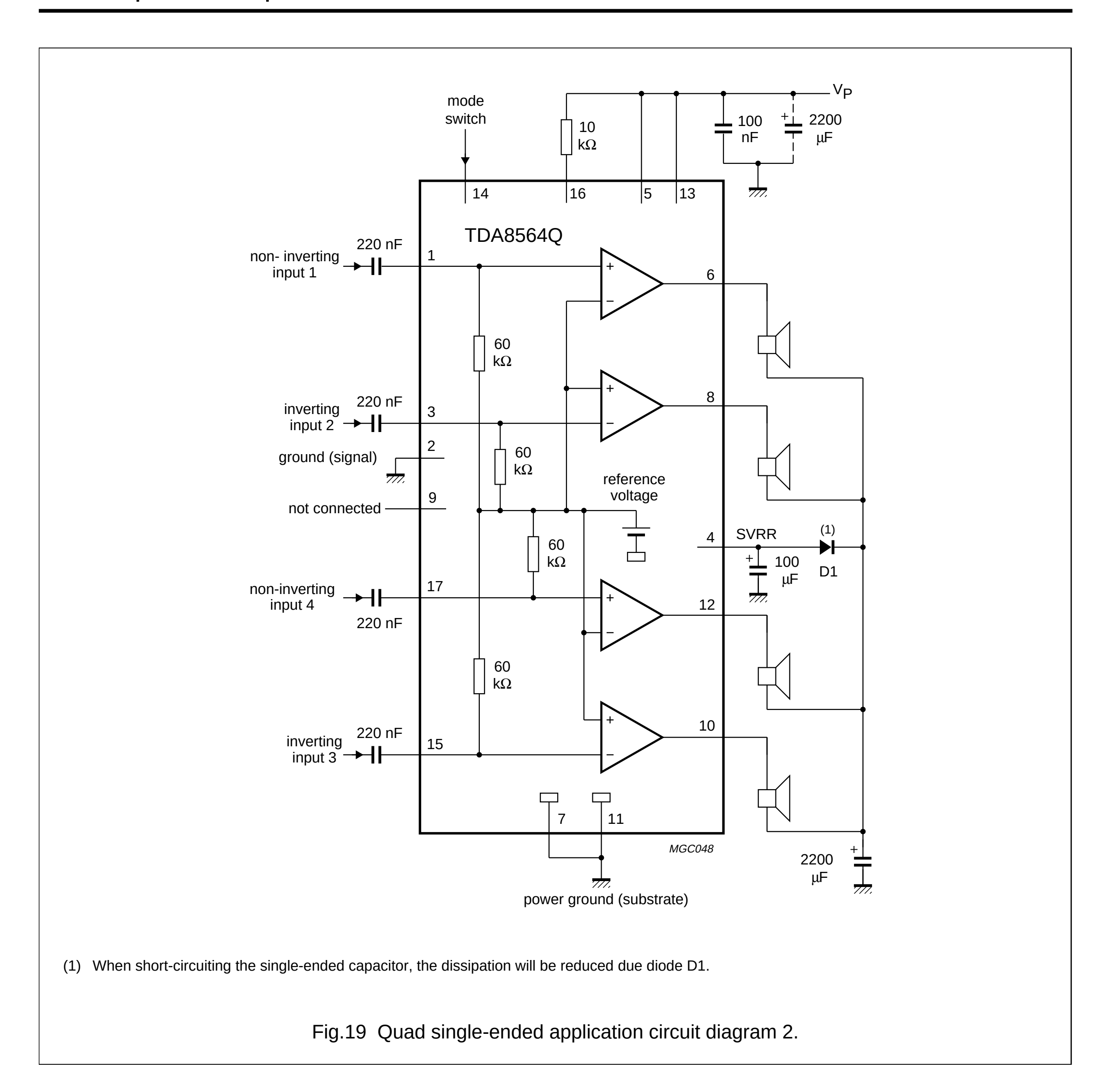


Fig.18 Quad single-ended application circuit diagram 1.



(1) When short-circuiting the single-ended capacitor, the dissipation will be reduced due diode D1.

Fig.19 Quad single-ended application circuit diagram 2.